WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a layer of insulation material formed over a semiconductor substrate; and

a metal trace formed in the layer of insulation material, the metal trace having a base region and a plurality of spaced-apart fingers that extend away from the base region.

2. The semiconductor device of claim 1 wherein the metal trace has a first end electrically connected to a first circuit, and a second end electrically connected to a second circuit, the metal trace passing a gigahertz-frequency signal from the first circuit to the second circuit.

3. The semiconductor device of claim 2 wherein the metal trace lies substantially in a plane horizontal to a surface of the substrate.

4. The semiconductor device of claim 2 wherein the fingers extend away from a bottom surface of the base region.

5. The semiconductor device of claim 2 wherein the metal trace is connected to a contact.

6. The semiconductor device of claim 2 wherein the metal trace is connected to a via.

7. The semiconductor device of claim 1 wherein the metal trace forms a number of loops.

8. The semiconductor device of claim 7 wherein the loops lie substantially in a same plane.

9. The semiconductor device of claim 7 wherein the metal trace has a first end and a second end.

10. The semiconductor device of claim 9 wherein the second end is connected to a contact.

11. The semiconductor device of claim 9 wherein the second end is connected to a via.

12. The semiconductor device of claim 11 wherein the via lies under the metal trace.

13. The semiconductor device of claim 7 wherein the fingers extend away from a bottom surface of the base region.

14. A method of forming a semiconductor device, the method comprising the steps of:

forming a layer of insulation material over a semiconductor substrate, the layer of insulation material having a top surface;

etching the layer of insulation material to form a plurality of first trenches in the layer of insulation material, the trenches having a first bottom surface vertically spaced a first distance apart from the top surface;

etching the layer of insulation material to form a second trench in the layer of insulation material, the second trench having the plurality of first trenches, the first trenches having a second bottom surface

vertically spaced a second distance apart from the top surface, the second distance being greater than the first distance;

forming a layer of conductive material on the layer of insulation material to fill up the second trench and the first trenches; and

planarizing the layer of conductive material to form a trace.

15. The method of claim 14 wherein the second etching step includes the steps of:

forming a layer of masking material on the layer of insulation material;

patterning the layer of masking material to expose the plurality of trenches;

anisotropically etching the layer of masking material to form the second trench.

16. The method of claim 14 wherein the trace is formed to have a number of loops.

17. The method of claim 15 wherein the loops lie substantially in a same plane.

18. The method of claim 14 wherein the trace is connected to a contact.

19. The method of claim 14 wherein the trace is connected to a via.

20. The method of claim 14 wherein the layer of conductive material includes:

a layer of barrier material formed on the layer of insulation material;

a layer of seed material formed on the layer of barrier material; and

a layer of copper formed on the layer of seed material.